IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Suresh Marisetty et al.

Title: ERROR CORRECTION APPARATUS, SYSTEMS, AND METHODS
Docket No.: 884.108US2 Serial No.: 10/628,726
Filed: July 28, 2003 Due Date: March 30, 2006
Examiner: Michael C. Maskulinski Group Art Unit: 2113

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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(GENERAL)

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REPLY BRIEF UNDER 37 C.F.R. § 41.41

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APPELLANT'S REPLY BRIEF

This Reply Brief is filed in response to the Examiner's Answer (hereinafter, the "Answer"), mailed January 30, 2006, and supplements the Appeal Brief filed by the Appellant on December 1, 2005. Please charge any required additional fees or credit overpayments to Deposit Account 19-0743.

Argument

The Appellant has reviewed the Answer, and believes the statements in the original Appeal Brief remain accurate and compelling. In responding to the Answer, the Appellant would like to further explore a selected few of the points raised by the Office. The corresponding section in the Answer, and page numbers, will be used to reference each of these points.

The Claimed Article of Manufacture Constitutes Patentable Subject Matter (Sect. 10, pg. 15):

The Office makes the statement that a "system and executable code may be an article of manufacture and a machine, but it is not necessarily true vice versa. A machine is not always a computer and a machine-accessible medium can be a piece of paper being scanned." The Appellant agrees. However, either situation makes no difference with respect to a rejection under 35 U.S.C. § 101.

As stated by the Office guidelines for examination, "[i]n many instances it is clear within which of the enumerated categories a claimed invention falls. Even if the characterization of the claimed invention is not clear, this is usually not an issue that will preclude making an accurate and correct assessment with respect to the section 101 analysis. The scope of 35 U.S.C. § 101 is the same regardless of the form or category of invention in which a particular claim is drafted. AT&T, 172 F.3d at 1357, 50 USPQ2d at 1451 . See also State Street, 149 F.3d at 1375, 47 USPQ2d at 1602 wherein the Federal Circuit explained

> The question of whether a claim encompasses statutory subject matter should not focus on which of the four categories of subject matter a claim is directed to -- process, machine, manufacture, or composition of matter -- [provided the subject matter falls into at least one category of statutory subject matter] but rather on the essential characteristics of the subject matter, in particular, its practical utility."

Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility, pg. 15, October 2005.

In addition, it is respectfully noted that "[w]hile abstract ideas, natural phenomena, and laws of nature are not eligible for patenting, methods and products employing abstract ideas, natural phenomena, and laws of nature to perform a real-world function may well be. In evaluating whether a claim meets the requirements of section 101, the claim must be considered as a whole to determine whether it is for a particular application of an abstract idea, natural phenomenon, or law of nature, rather than for the abstract idea, natural phenomenon, or law of nature itself." *Id.* at pgs. 17-18. The Appellant's claimed article of manufacture, comprising a machine-accessible medium having associated data, which when accessed, results in a machine performing a series of activities (e.g., attempting to correct an error ..., on failure, executing firmware code ... to correct the error, and on failure, entering a rendevous state ..." is clearly a practical application that achieves a useful, concrete, and tangible final result, as defined in the guidlines. *See Id.* at pgs. 20-22. Therefore, claims 24-26 constitute patentable subject matter, and the rejection of these claims under 35 U.S.C. § 101 is improper.

Neither Bowers' Controller nor Falik's Debugger Operates as a Monarch Processor (Sect. 10, pgs. 15-18):

While claims during examination should be interpreted as broadly as their terms reasonably allow, that interpretation must be tempered by the context in which the terms are used. The *Hyatt* court states that "during examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2D (BNA) 1664, 1667 (Fed. Cir. 2000) (emphasis added) ("During examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification."; citing *In re Graves*, 69 F.3d 1147, 1152, 36 U.S.P.Q.2D (BNA) 1697, 1701 (Fed. Cir. 1995); *In re Etter*, 756 F.2d 852, 858, 225 U.S.P.Q. (BNA) 1, 5 (Fed. Cir. 1985) (en banc).).

The interpretation of the term "monarch processor" proffered by the Office is neither reasonable, nor consistent with the specification. It is not reasonable because it contradicts the meaning of the term as understood by those of skill in the art. For example, some in the industry note that "[w]hen the monarch processor is selected, the remaining ("serf") processors go into the "rendezvous code" where all interrupts are cleared. ... If the monarch fails, the serfs can usurp its power (deconfigure the monarch) and force a system reboot, whereupon the arbitration process is repeated and a new monarch selected." HP-UX MultiProcessing White Paper, Version 1.3, 5965-4643, April 7, 1997. Neither the controller of Bowers, nor the debugger of Falik are capable of operating in this fashion, since this would mean that the controller or the debugger could be replaced by one of the other processors, and vice versa.

The interpretation by the Office is also not consistent with the specification, which states "The monarch processor is one of the plurality of processors 104. The monarch processor can simply be selected as the processor that detected the error. Or, the detecting processor can execute a SAL 102 routine to select a processor to be the monarch processor based on certain criteria. The criteria could be which processor is unaffected by the error or which one can most efficiently correct the error. Lastly, the monarch processor could pre-designated by design or on system startup." Application, pg. 8, lines 17-23. Thus, the attempt by the Office to characterize

Bowers or Falik as teaching a "monarch processor" is beyond that which should be reasonably allowed, and the rejection of claims 5-16, 18-19, and 24-26 under 35 USC § 102(b) is improper.

Appellant's Arguments Comply with 37 CFR 1.111(b) (Sect. 10, pg. 17):

The Office asserts that the Appellant's arguments do not comply with 37 CFR 1.111(b) because "the Appellant's arguments ... amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." In reply, instead of duplicating the language of the Appeal Brief, the Appellant simply notes that pg. 15 of the Brief recites specific elements of each rejected claim that are not taught by Bowers and Falik. Therefore, the Appellant's arguments do indeed comply with 37 CFR 1.111(b).

A Debugger, Without More, Does not Correct Errors (Sect. 10, pg. 19):

The Office states that "[t]he Appellant's assertion that a human is involved in the debugging process of Falik is not supported by Falik ..." is somewhat misleading. As noted in the Appeal Brief, Falik's debugger, or a monitor, are the only resources described by the reference. Neither of these items, as understood by those of ordinary skill in the art, operate independently to "correct the error." For example, according to Microsoft's Developer Network Library, at http://msdn.microsoft.com/library/default.asp?url=/library/en-us/debug/base/debugging_terminology.asp, a debugger is "[a] program designed to help detect, locate, and correct errors in another program. It allows the developer to step through the execution of the process and its threads, monitoring memory, variables, and other elements of process and thread context." Thus, a debugger assists a human to accomplish these functions. Falik provides no evidence of automating such activities. The assertion by the Office that the "debugger appears to be a software program that is capable of correcting errors," implying that such occurs without human intervention, does not constitute evidence, and attributing such an operation to Falik's debugger goes beyond what is reasonably understood by those of skill in the art. Therefore, Falik does not teach "correcting the error" as claimed by the Appellant.

Falik Teaches at Least Two Processors Must Be Awake (Sect. 10, pg. 20):

The Office is "unsure as to where the Appellant gets the notion that at least two processors must be operational." It is respectfully noted that Falik requires two processors to be awake because the debugger 1830 only operates by communicating with the monitor in each one of the processors. *See* Falik, Col. 2, lines 37-43. With respect to the Office assertion that "[i]t is clear that all of the monitors on the processors are brought back up and synchronized after the error is corrected ...", the Appellant notes that the key word is "after". That is, the process of correcting an error requires at least two processors (the debugger and one other processor) to be in communication, and only *after* such communication is effected can a reset be accomplished. In fact, as noted by Falik, if there is a lockout of the communication hardware, such that communication is lost with all processors, "executing a reset instruction is guaranteed to recover from all these locked cases, but this will have the impact of resetting the entire chip. These sequences should be avoided by the host." Falik, Col. 18, lines 39-48. "The debugger interface module 1841 provides a debugger reset request signal to the reset circuit, which in response provides a reset signal to the entire chip, including the debugger interface module 1841. Falik, Col. 2, lines 59-62. Thus, Falik teaches maintaining minimal communication between the debugger (one processor) and one of the processors (another processor) so that the debugger can operate. A reset instruction results in resetting all processors, as well as the debugger interface, so that no communication (to correct an error) is possible.

The Use of Routine Maintenance Does Not Indicate that Something is Wrong (Sect. 10, pg. 21):

The Office asserts that to "replace a processor for routine maintenance indicates that there is something wrong with the processor ...". However, it is respectfully noted that the term routine maintenance, as such is commonly understood, refers to work that is conducted on a periodic basis to keep systems operating without breaking down. For example, the government of Australia offers the following definition: "Regular progress of works to prevent deterioration of the asset's capability e.g.; service to power generation." *A Report to the ANZECC Working Group on National Park and Protected Area Management*, Department of Environment and Natural Resources, South Australia 1997. Clearly, "routine" maintenance is exactly that; maintenance carried out as a matter of routine, and not because "there is something wrong." To the contrary, routine maintenance is performed so that breakdowns may be averted. For

example, if the MTBF (mean-time between failures) for a processor is 10,000 hours, and the processor has been operating for 9,000 hours, it may be prudent, as a matter of routine maintenance, to replace the processor, even though no specific errors are in evidence. In this manner, on average, another 9,000 hours of error-free operation may be anticipated.

In addition, Bowers teaches other reasons to replace processors. For example, "[t]o replace a processor, it currently must be taken out of service temporarily. This may cause loss of information and of configuration, and it typically requires the system to be rebooted. Depending upon the redundancy and complexity of the computer system, such a temporary removal may have wide ranging effects, from slightly degrading the overall performance of the computer system to temporarily removing the computer system from service. This problem is exacerbated by the fact that it is typically desirable to upgrade a computer's processors from time to time. Such upgrades must typically be scheduled during non-peak times in order to minimize the downtime or performance degradation of the networked computer system." Bowers, Col. 2, lines 25-37. Thus, the fact that routine maintenance is performed to replace a processor does not indicated that something is wrong with the processor. Such activity may be performed simply to update/upgrade the system capabilities.

A Severe Error is Not the Same as a Non-Recoverable Error (Sect. 10, pg. 21):

This is again a case where the interpretation offered by the Office is inconsistent with what is stated in the Application. As noted in the Appeal Brief and the Application, a severe error "is generally corrected by entering the rendezvous state." *See* Application, pg. 7, lines 19-24. Thus, a severe error is generally a correctable error, and should not be confused with the non-recoverable error described by Fujii.

Bowers is Concerned with Replacing Processors and Only That (Sect. 10, pg. 22):

While Bowers may be directed toward replacing processors, this teaching does not negate the fact that other components may be the cause of errors in a computing system. Thus, simply knowing the severity of an error does not immediately indicate how it should be corrected. Therefore, the Examiner appears to be relying on personal knowledge to support the assertion that "knowing the severity of the error determines what action should be taken (e.g., removal of a

processor) ...". Given this set of circumstances, it is again respectfully requested that the Examiner submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

There is no Motivation to Combine Bowers and Fujii (Sect. 10, pg. 23):

While the Office continues to argue that this combination should be made, it has already been noted in the Appeal Brief that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. In this case, the suggested combination prevents attaining the objectives sought by the cited references, and/or provides no reasonable expectation of success, and is therefore undesirable. Therefore, the Appellant maintains that no motivation exists to combine Bowers and Fujii, and the rejection of claim 17 under 35 USC § 103(a) is improper.

Conclusion

It is respectfully submitted that no *prima facie* case of the existence of nonstatutory subject matter under 35 U.S.C. §101, nor of anticipation under 35 U.S.C. §102, nor of obviousness under 35 U.S.C. §103 has been established by the Office. Therefore, it is respectfully requested that the rejections of claims 5-19 and 24-26 be reconsidered and withdrawn.

The Appellant respectfully submits that all of the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellant's attorney, Mark Muller at (210) 308-5677, or the undersigned attorney at (612) 349-9592, to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SURESH MARISETTY ET AL.

By their Representatives,

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Chris Hammond
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Chi Hammond
Signature